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SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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08/484,935 06/07/95 MOORE

C NANO-001/09U

ENG. D. EXAMINER

E3M1/1207

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ART UNIT PAPER NUMBER

2315

#5

DATE MAILED: 12/07/95

This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to communication filed on 6/7/95 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 3 days from the date of this letter.  
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- |   |  |
|---|--|
| 1. <input checked="" type="checkbox"/> Notice of References Cited by Examiner, PTO-892. | 2. <input checked="" type="checkbox"/> Notice of Draftsman's Patent Drawing Review, PTO-948. |
| 3. <input type="checkbox"/> Notice of Art Cited by Applicant, PTO-1449.                 | 4. <input type="checkbox"/> Notice of Informal Patent Application, PTO-152.                  |
| 5. <input type="checkbox"/> Information on How to Effect Drawing Changes, PTO-1474.     | 6. <input type="checkbox"/>  |

Part II SUMMARY OF ACTION

1. ☒ Claims 71-85 are pending in the application.  
Of the above, claims \_\_\_\_\_ are withdrawn from consideration.
2. ☒ Claims 1-20 have been cancelled.
3. ☐ Claims \_\_\_\_\_ are allowed.
4. ☒ Claims 71-85 are rejected.
5. ☐ Claims \_\_\_\_\_ are objected to.
6. ☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on \_\_\_\_\_. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on \_\_\_\_\_, has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed \_\_\_\_\_, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. \_\_\_\_\_; filed on \_\_\_\_\_.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

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The preliminary amendment filed on June 7, 1995 has been entered. Claims 1-70 have been cancelled. The active claims are 71-85.

Applicants are requested to update the status of parent application.

A new title and a new abstract which are more aptly descriptive of the invention claimed are requested.

Claims 71-85 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 71 recites that the instructions are fetched for the CPU. However, none of the instructions are supplied to the CPU. Further with respect to claim 71, it is not clear how the instruction supplying means and the counter as recited functionally coact with each other. It appears that supplying instruction from one element to another does not require counting pulses from a counter.

Function of the skip instruction recited in claims 72 and 73, the loop instruction recited in claims 74-76, the variable-length-operand-using instruction recited in claim 77, the last-byte-operand-using instruction as recited in claim 78, the extra-group-operand-using instruction as recited in claim 79, the

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branch-type instruction as recited in claims 82-83 is not clear. No meaningful result is seen from the execution of those instructions.

The claims fail to recite sufficient structural means for supporting the functional language set forth therein. See claim 78 for example. A decoder which is commonly for decoding instruction is unable to perform the operation as recited in claim 78.

The following have no clear antecedent basis:

1. "said response to a SKIP instruction" in claim 73.
2. "the testing of a condition" in claim 73.
3. "'said branch-type instruction" in claim 81/77/71.

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

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Claims 71-73, 78-80 and 82-85 are rejected under 35 U.S.C. § 103 as being unpatentable over Boufarah.

See at least Figures 1 and 3 in Boufarah. Boufarah teaches a microprocessor system comprising:

a cpu 20,  
a memory 10,  
a bus,  
instruction fetching means 14,  
an instruction register 34, 36 and 38,  
instruction supplying means 14,  
a counter (inherent program counter),  
instruction decoding means (processors 20 and 22).

With respect to claims 72-73, Boufarah also includes instructions for controlling the fetching means 14 to fetch subsequent instructions.

With respect to claims 78-79, Boufarah's processor is also capable of executing instructions having operands.

With respect to claims 80-83 see Figures 3 in Boufarah.

With respect to claim 84, see claim 2 in Boufarah.

With respect to claim 85, memory access instruction is well known in the art.

Boufarah does not explicitly show a decoder. One of ordinary skill in the art should readily recognize that decoder is an inherent component in a processor.

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Claims 74-77 and 81 are rejected under 35 U.S.C. § 103 as being unpatentable over Boufarah in view of May.

Boufarah discloses claim combination set forth above. Boufarah does not teach loop instruction and variable length operand instruction. However, May teaches system for executing loop instructions (see "jump" at the bottom of column 15~~0~~ and variable length operand instruction (See brief description of Figure 8 and column 21). May further teaches SKIP at the top of column 16. Since both references are directed toward instruction execution, it would have been obvious to a person of ordinary skill in the art to incorporate the instructions of May in the Boufarah's system because that would make the system more efficient.



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PRIMARY EXAMINER  
ART UNIT 232